Track A (Active): 2-GHz band high efficiency power amplifier design competition

Requirement for applicants: students

1. Evaluation

The maximum power added efficiency of the fabricated power amplifier is evaluated, when inputting CW signal with the IMT band 1 (2.110GHz to 2.170GHz). The measurement frequency and input power level are decided by the attendee.

2. Conditions

(a) The power amplifier must be single stage.

(b) The attendee can only employ commercial available transistors, and do not employ internal-matched type transistors and MMICs. Do not disclose the number and type of the transistors. The attendee must buy the transistors by yourself.

(c) The maximum output power level of the power amplifier must be less than 30 dBm by the CW test.

(d) The minimum input power level of the power amplifier must be more than -20 dBm by the CW test.

(e) The voltage and current of the drain bias are less than 50 V and less than 1 A, or less than 18 V and less than 3 A. The voltage and current of the gate bias are from -10 V to 10 V and less than 1 A.

(f) The connectors of input and output ports of the power amplifier must be female SMA connectors which are ISO metric screw threads. Do not use inch size connectors.

(g) The power amplifier must not oscillate when applying the gate and drain voltages.

3. Experimental Environments on Site

The following pieces of equipment will be prepared by the SDC committee for the evaluation at the competition:

- A network analyzer
- A power supply for drain bias with 50 V and 1 A
- A power supply for drain bias with 18 V and 3 A
- A power supply for gate bias with 10V and 1A